4-18-00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

The Commissioner of Patents and Trademarks
Washington, D.C. 20231

Date: April 17, 2000
Docket No. YOR9-1996-0118US3
Prior Art Unit: 2814
Prior Examiner: D. Wille

Sir:

This is a request for filing a [ ] continuation [X] divisional [ ] continuation-in-part, under 37 C.F.R. **1.53(b)** of pending prior application Serial No. 09/107,738 filed on June 30, 1998 of K.K. Chan et al. for A SCALABLE MOS FIELD EFFECT TRANSISTOR which is a continuation-in-part application of application Serial No. 08/683,329 filed on July 18, 1996 of K.K. Chan et al.

1. [ ] As last amended, the title has been changed to _____.
2. [ ] As last amended, the name of applicant has been changed to_____.
3. [X] Enclosed is [X] a copy of the specification and Preliminary Amendment filed as a CIP and the oath or declaration as filed in the prior application or [ ] a new oath or declaration.
4. [X] The filing fee is calculated below:

CLAIMS AS FILED IN THIS APPLICATION	NUMBER FILED				NUMBER EXTRA		RATE		BASIC FEE
								=	$690.00
TOTAL CLAIMS	22	-	20	=	2	X	$18.00	=	$36.00
INDEPENDENT CLAIMS	3	-	3	=	0	X	$78.00	=	
[ ] MULTIPLE DEPENDENT CLAIMS, (IF ANY)								=	
TOTAL FILING FEE								=	$726.00

5. [X] Charge any fees which may be required, except for the Issue Fee, or credit any overpayment to Deposit Account No. 09-0468.
6. [X] Cancel in this application original Claims 1-8, 13-21, 24-29, 34-36, 44-57, and 61-62 of the prior application before calculating the filing fee.
7. [X] Amend the specification by inserting before the first line the sentence: - This is a [ ] continuation [X] division [ ] continuation-in-part, of application Serial No. 09/107,738 , filed June 30, 1998, which is a continuation-in-part application of application Serial No. 08/683,329 filed on July 18, 1996.
8. [ ] Priority of application Serial No. _____ ,filed on _____ in _____ is claimed under 35 U.S.C. 119.
9. [ ] The certified copy of the priority application has been filed in prior application Serial No. _____ filed _____.
10. [ ] An appointment of associates is enclosed.
11. [X] Address all future communications to Robert M. Trepp, IBM Corporation, Intellectual Property Law Dept., P.O. Box 218, Yorktown Heights, N.Y. 10598.
12. [X] A preliminary amendment to this application is enclosed.
13. [ ] Enter in this application the amendment under 37 C.F.R. 1.116 which was unentered in the prior application.

Robert M. Trepp

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Atty. Docket No. YOR9-1996-0118US3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: K.K. Chan et al.

Serial No. Group Art Unit:

Filed: (Herewith) Examiner:

For: A SCALABLE MOS FIELD EFFECT TRANSISTOR

Assistant Commissioner of Patents and Trademarks
Washington, D.C. 20231

EXPRESS MAIL CERTIFICATE

"Express Mail" label number: EL549238545US

Date of Deposit: April 17, 2000

I hereby certify that the following **attached** paper or fee

Request for filing a Divisional Application Under 37 CFR 1.53(b)
Copy of original patent application, as filed, and copy of Preliminary Amendment filed on June 30, 1998, which together comprise the CIP
Copy of original drawings (8 sheets), as filed
Copy of original Declaration and Power of Attorney
Preliminary Amendment
Information Disclosure Statement Under 37 CFR 1.97(b)(1)
Copy of PTO-1449 Form (2 sheets) filed on June 30, 1998 and February 16, 2000
Acknowledgment Card

is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Sandra M. Emma
(Typed or Printed name of person mailing paper)

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In re Patent Application of :

Kevin K. Chan et al. : Group Art Unit: 2503

S.N. To be assigned :

Filed: Herewith : Examiner: S. Meier

For: A Scalable MOS Field Effect Transistor

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents
Washington, D. C. 20231

Sir:

Please amend the prior application, Serial No. 08/683,329, as follows:

In the Specification

Page 2, line 11, change "width" to --gate length--; same line, after "scaled" insert --to smaller dimensions--.

Page 6, after line 13, insert

--Fig. 21 shows a schematic view of an electrochemical anodic oxidation set-up.

Fig. 22 shows a top view of several gate oxide regions during a step in fabricating a sixth embodiment of the invention.

Fig. 23 shows a cross section view of a sixth embodiment of the invention.

Fig. 24 shows a cross section view of a seventh embodiment of the invention.

Fig. 25 shows a cross section view of an eighth embodiment of the invention.--.

Page 8, line 17, change "4" to --5--.

Page 8, line 23, change "sacrificiaal" to --sacrificial--.

Page 9, line 9, change "oxide" to --dielectric--.

Page 9, line 11, change "Gate oxide 26 may" to --Gate dielectric 26 may be, for example, silicon oxide, silicon nitride, silicon oxynitride, or a silicon oxide/silicon nitride composite, and may--.

Page 9, line 12, after "20" insert --nm--.

Page 9, line 16, change "oxide" to --dielectric--.

Page 9, line 18, change "sacrificial" to --insulating--; same line, change "14" to --18--; same line, change "oxide" to --dielectric--.

Page 9, line 21, change "oxide", second occurrence, to --dielectric--.

Page 10, line 2, change "co planar" to --coplanar--.

Page 11, line 9, change "atoms/cm3" to --atoms/cm^3--.

Page 11, line 18, change "oxide" to --dielectric--.

Page 11, line 22, change "oxide" to --dielectric--.

Page 12, line 1, change "oxide" to --dielectric--.

Page 12, line 7, change "titanium or platinum" to --Al, Er, Hf, Nb, Pt, Ta, Ti, Y, W or Zr--.

Page 12, after line 15, insert two new paragraphs --The oxidation process for oxidizing metal layer 16 in gate window 19 to form gate dielectric 50 may be thermal. In this case, insulating layer 18 must also act as a diffusion barrier to oxygen to prevent oxidation of the source/drain metallurgy, metal layer 16 beneath insulating layer 18. A preferred material for insulating layer 18 would be silicon nitride. SiO_2 is not as preferred as a material since it is typically too permeable to ambient oxygen during oxidation.

Gate dielectric 50 may alternatively be formed by an electrochemical anodic oxidation process, such as described in Handbook of Thin film Technology, by Maissel and R. Glang, McGraw Hill (1983), chapters 5 and 19. Electrochemical anodic oxidation of metal layer 16 in gate window 19 may be used to produce metal oxides which may be for example Al_2O_3, Er_2O_3, HfO_2, Nb_2O_5, PdO, PtO, Ta_2O_5, TiO_2, WO_3, Y_2O_3 and ZrO_2 from respective metals Al, Er, Hf, Nb, Pd, Pt, Ta, Ti, W, Y and Zr. Some of the above metals may form oxides other than those listed above. Furthermore, some of the above mentioned metal oxides such as PdO and PtO may be less preferred due to their relatively high conductivities. The other oxides listed above are preferred. Relative to thermal oxidation, electrochemical anodic oxidation processes have the advantages of (i) lower processing temperature in the range where the electrolyte is in the liquid phase, typically from about 0°C to about 100°C, (ii) greater spatial selectivity, in that oxidation will only begin on metal surfaces directly in contact with the electrolyte, and (iii) easier process control over uniformity and endpoint. For example, control over process uniformity may be easier because the maximum metal oxide film thickness can be set by the applied voltage, instead of by the time integral of an average current density that may show strong local variations. This self-limiting aspect of oxide formation thus makes it easier to make a uniform oxide over a wider variety of pattern densities and feature sizes. Additional process parameters influencing oxide quality and

thickness include the metal type and purity, and the electrolyte composition and temperature.

Gate dielectric 50 may alternatively be formed in gate window 19 by a reaction of metal layer 16 and a gaseous plasma to produce an oxide, nitride or oxynitride. Formation of gate dielectric 50 by the process of electrochemical anodic oxidation, plasma oxidation or plasma nitridation may further include one or more subsequent thermal treatments, for example, heating in a reactive or nonreactive ambient to a temperature above a selected temperature.--.

Page 13, line 4, delete "or on gate dielectric 26".

Page 13, line 14, after "." insert two new sentences, --After formation of epitaxial channel layer 52, a gate dielectric 26 is formed over channel layer 52, the sidewalls of gate window 19, and on the upper surface of insulating layer 18. A T-shaped gate 32 of gate material 30 is formed over gate dielectric 26.--.

Page 14, line 8, change "oxide" to --dielectric--.

Page 14, after line 25, insert several new paragraphs,--A schematic of an electrochemical anodic oxidation set-up to form the structure of Fig. 15 is shown in Fig. 21. The electrochemical cell consists of housing 63 containing electrolyte solution 64, a working piece such as metal layer 16 acting as electrode 67, and counter electrode 68 positioned in electrolyte solution 64 spaced from metal layer 16. Electrolyte solution 64 may be for example concentrated HNO_3, 0.1% to 10% citric acid, or about 10% acetic acid. Insulating layer 18 protects underlying metal layer 16 of regions that will become the source/drain 74 metallurgy.

Fig. 22 illustrates a top view of several gate oxide regions 50 in respective gate windows 19 surrounded by insulating layer 18 and still-connected metal layer 16 below insulating layer 18 which will be subsequently patterned to form source/drain 74 contact regions on either side of gate oxide 50. Metal layer 16 on substrate 1 may be used as the electrode throughout the anodization process since the gate oxide regions 50 in respective gate windows 19 are always formed as isolated islands that do not interfere with the connectedness of the surrounding source/drain 74 electrode metal.

T-shaped gate structures incorporating a gate oxide or nitride formed by oxidation or nitridation of an in-situ metal layer 16 need not be limited to the device geometry shown in Fig. 16. For

example, the source/drain metallurgy may consist of a bottom metal layer 16 which is locally oxidized or nitridized in gate window 19 to form gate dielectric 50. One or more conductive layers of low resistance material may be formed over metal layer 16 to reduce the source/drain resistance.

Fig. 23 shows an embodiment of a field effect transistor 76 containing a double layer source/drain metallurgy comprising bottom layer 16 and top layer 78. Gate dielectric 50 is a metal oxide, nitride, or oxynitride of the metal used for bottom layer 16. Insulating sidewall layers 79 in the gate window may be formed on the sidewalls of top layer 78 before, during or after formation of gate oxide 50, by a process such as thermal oxidation, electrochemical anodic oxidation, plasma oxidation, plasma nitridation, or combinations thereof, to electrically isolate layer 78 from subsequently formed T-shaped gate 32. A second layer of low resistance material 80 may be formed over gate material 30 prior to patterning to form T-shaped gate 32.

The embodiment in Fig. 23 has the advantage that upper conductive material 78 may be selected for its low resistivity while bottom conductive material 16 may be selected for the electrical qualities of its oxide or nitride dielectric, its Schottky barrier properties, and its compatibility with the underlying substrate material 1. Metal layer 16 should preferably be thin to enable complete oxidation of metal layer 16 with a minimum of oxidation

under layer 78 at the edges of gate window 19, to avoid increasing the gate length of transistor 76.

An alternative to the insulating sidewall layers 79 is shown in Fig. 24, where field effect transistor 82 contains a double layer source/drain metallurgy comprising bottom layer 16 and top layer 78. As in Fig. 23, gate dielectric 50 is a metal oxide, nitride, or oxynitride of the metal used for bottom layer 16. Insulating sidewall spacers 84 are formed by conformally depositing a thin dielectric layer on metal layer 16 in gate window 19, sidewalls of conductive material 78 in gate window 19, and upper surface of insulating layer 18, and then anisotropically etching said thin dielectric layer by a process such as reactive ion etching (RIE) to produce sidewall spacers 84. Metal layer 16 in the gate window 19 may also be etched to reduce thickness and to clean the surface prior to oxidation or nitridation.

The bottom metal layer 16 should ideally not react with or consume the underlying semiconductor substrate 1, and should act as a barrier against the reaction of the upper conductive layer 78 with substrate 1. An example of a suitable bottom layer 16/top layer 78 combination is Ta/Al. Ta is a good barrier material and forms an excellent Ta_2O_5 gate oxide. However, the resistivity of Ta in its thin film beta phase form is 170 micro-ohm-cm which is too high for it to be used alone as a source/drain contact metal. In contrast,

Al has a low resistivity. However, without a material such as Ta to act as a barrier to such reaction, the Al may react with substrate material 1 during anneals required in subsequent process steps in forming an integrated circuit.

Fig. 25 shows another field effect transistor structure 88 having the same double layer source/drain metallurgy as the structures 76 and 82 in Figs. 23 and 24. Dielectric 90 replaces gate dielectric 50 and sidewall insulators 79 or 84 shown in Fig. 24, and is deposited in gate window 19, on the sidewalls of conductive material 78 in gate window 19, and on upper surface of insulating layer 18. Dielectric 90 may be a deposited silicon oxide, silicon nitride, or silicon oxynitride, or silicon oxide/silicon nitride composite or it may be an oxide, nitride, or oxynitride of a deposited metal layer, formed for example by deposition of Al, Er, Hf, Nb, Ta, Ti, W, Y, Zr and mixtures thereof and subsequent electrochemical anodic oxidation, thermal oxidation, gaseous plasma anodization, or combinations thereof.--.

In the Claims

23. (Amended) The field effect transistor of claim 22 wherein said heavily doped semiconductor regions include [SiGe alloy] a material selected from the group consisting of GaAs, InGaAs, InP, $In_{1-x}Ga_xAs_yP_{1-y}$ and SiGe.

Add new Claims:

37. The field effect transistor of claim 30 wherein said spaced apart metal-semiconductor compound regions further include an additional layer of conductive material between said metal and said first dielectric layer, said additional layer of conductive material having sidewalls, said sidewalls having an insulating material disposed thereon.

38. The field effect transistor of claim 37 wherein said additional layer of conductive material includes an oxidizable material.

39. The field effect transistor of claim 37 wherein said additional layer of conductive material is selected from the group consisting of Al, Co, Er, Ni, Pd, Pt, Rh, Ta, Ti and W.

40. The field effect transistor of claim 37 wherein said metal of said metal-semiconductor compound regions is selected from the group consisting of Al, Co, Er, Ni, Pd, Pt, Rh, Ta, Ti and W.

41. The field effect transistor of claim 37 wherein said two spaced apart metal-semiconductor compound regions include Ta and said additional layer of conductive material includes Al.

42. The field effect transistor of claim 37 wherein said insulating material disposed on said sidewalls of said additional layer of conductive material also covers sidewalls of said first dielectric layer.

43. The field effect transistor of claim 37 wherein said insulating material disposed on said sidewalls of said additional layer of conductive material includes an oxide of said additional conductive material.

44. A method of forming a field effect transistor comprising the steps of:

selecting a substrate of single crystal semiconductor material,

forming a metal layer on said substrate, said metal layer including material suitable for forming a Schottky metal-to-semiconductor barrier and having a selected work function,

forming an insulating layer over said metal layer,

forming a gate opening in said insulating layer to expose said metal layer,

forming a gate dielectric in said gate opening by oxidation of said metal layer,

forming a conductive layer on said gate dielectric in said gate opening, and

patterning said conductive layer to define a gate electrode,

said Schottky metal-to-semiconductor barrier on opposite sides of said gate electrode corresponding to the source and drain of said field effect transistor.

45. The method of claim 44 wherein said step of forming a gate dielectric by oxidation includes the step of electrochemical anodic oxidation of said metal layer.

46. The method of claim 44 wherein said step of forming a gate dielectric by oxidation includes the step of gaseous plasma anodization.

47. The method of claim 44 wherein said step of forming a gate dielectric by oxidation includes the step of heating said metal layer in a reactive ambient to a temperature above a selected temperature.

48. The method of claim 45 further including the step of heating said metal layer in an ambient to a temperature above a selected temperature.

49. The method of claim 46 further including the step of heating said metal layer in an ambient to a temperature above a selected temperature.

50. The method of claim 44 further including the step of forming an additional layer of conductive material over said metal layer after said step of forming a metal layer.

51. The method of claim 50 further including the step of forming an insulating material on exposed sidewalls of said additional layer of conductive material.

52. The method of claim 51 wherein said step of forming an insulating material includes the step of electrochemical anodic oxidation of exposed sidewall regions of said additional conductive material.

53. The method of claim 51 wherein said step of forming an insulating material includes the step of gaseous plasma anodization of exposed sidewall regions of said additional conductive material.

54. The method of claim 51 wherein said step of forming an insulating material includes the step of heating said conductive material in a reactive ambient to a temperature above a selected temperature.

55. The method of claim 52 further including the step of heating said conductive material in an ambient to a temperature above a selected temperature.

56. The method of claim 53 further including the step of heating said conductive material in an ambient to a temperature above a selected temperature.

57. The method of claim 51 wherein said step of disposing an insulating material includes the step of depositing a thin conformal layer of said insulating material in said gate opening and anisotropically etching said insulating material to form 37.

58 The field effect transistor of claim 9 wherein said spaced apart Schottky metal-semiconductor compound regions further include an additional layer of conductive material between said metal and said first dielectric layer, said additional layer of conductive

material having sidewalls, said sidewalls having an insulating material disposed thereon.

59. The field effect transistor of claim 58 wherein said insulating material includes an extension of said gate dielectric layer.

60. The field effect transistor of claim 58 wherein material of said gate dielectric layer is selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, silicon oxide/silicon nitride composites, and an oxide, nitride, or oxynitride of Al, Er, Hf, Nb, Ta, Ti, W, Y and Zr and mixtures thereof.

61. A method of forming a field effect transistor comprising the steps of:

selecting a substrate of single crystal semiconductor material,

forming at least one conductive layer on said substrate, said at least on conductive layer including a metal suitable for forming a Schottky metal-to-semiconductor barrier and having a selected work function,

forming an insulating layer over said at least one conductive layer,

forming a gate opening in said at least one conductive layer and said insulating layer,

forming a gate dielectric in said gate opening,

forming a second conductive layer on said gate dielectric in said gate opening, and

patterning said second conductive layer to define a gate electrode,

said Schottky metal-to-semiconductor barrier on opposite sides of said gate electrode corresponding to the source and drain of said field effect transistor.

62. The method of claim 61 further including the step of forming an insulating material on exposed sidewalls of said at least one layer of conductive material.

63. The field effect transistor of claim 9 further including a raised epitaxial channel on said substrate, said raised epitaxial channel formed between said Schottky metal semiconductor compound regions forming said source and drain.

64. The field effect transistor of claim 22 further including a raised epitaxial channel on said substrate, said raised epitaxial channel formed between said semiconductor regions forming said source and drain.

DRAWING

Enclosed is the drawing consisting of sheets 1-8 containing Figs. 1-25. Sheets 1-6 were in the prior application and contained Figs. 1-20. Sheets 7 and 8 are new and contain Figs. 21-25.

REMARKS

An inventor, Katherine L. Saenger, has been added to the named inventors of this application.

Enclosed is a copy of the prior specification as filed in the parent application.

Several typographical errors have been corrected in the specification.

New material has been added to the specification to expand the scope of the invention.

Sheets 7 and 8 containing Figs. 21-25 have been added to the drawing of the prior application which consisted of sheets 1-6.

Claim 23 has been amended to conform with amended claim 23 in the prior application.

New claims 37-62 have been added to claim additional subject matter added to the specification by the instant continuation-in-part application.

Claims 37 and 38 submitted by amendment in the prior application now correspond to claims 63 and 64 respectively.

Enclosed is an Information Disclosure Statement containing a copy of PTO form 1449 submitted in the prior application.

Further favorable action and allowance of the claims is earnestly requested.

Respectfully submitted,

Robert M. Trepp, Attorney
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Date: April 17, 2000

K.K. Chan et al. Group Art Unit:

Serial No. Examiner:

Filed: (Herewith) Docket No.YOR9-1996-0118US3

For: A SCALABLE MOS FIELD EFFECT TRANSISTOR

Assistant Commissioner of Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified application as follows:

IN THE SPECIFICATION

In the Preliminary Amendment which was filed June 30, 1998 as part of the CIP (amending the specification on page 12 after line15), page 4, line 3, after "by" insert --L.I.--; same line delete "McGraw".

In the Preliminary Amendment (amending the specification on page 12 after line 15), page 4, line 4, change "Hill (1983)" to --McGraw-Hill, Inc. (1970)--.

REMARKS

The specification at page 12 after line 15 has been amended to correct typographical errors which are on page 4 of the Preliminary Amendment.

Favorable further action is earnestly requested.

Respectfully submitted,

Robert M. Trepp
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Express Mail Label No.: EM541215234US
Date of Deposit: July 18, 1996

A Scalable MOS Field Effect Transistor

Field of the Invention

This invention relates to semiconductors and more particularly to self aligned metal oxide semiconductor (MOS) field effect transistors (FET's) having submicron gate lengths with a T-shaped gate.

Background of the Invention

State-of-the-art metal-oxide-semiconductor field effect transistors require shrinking the gate length below 0.25μm. The standard process for forming the gates is by depositing a polysilicon layer, etching this layer to define the required gate length, and using the polysilicon as a mask for the source/drain shallow implant step. The shallow implant step is followed by forming a nitride sidewall spacer, implanting the deep ohmic region in the source/drain and then forming a metal silicide to the gate and the source/drain implant. The resistance of the gate thus increases as the gate length is reduced, because the gate metal silicide has the same gate length as the polysilicon gate underneath. The gate resistance slows down the devices because of the RC time delay. Alternatively, one can form a metal gate which

is longer than the polysilicon gate by opening a window in an oxide layer and patterning metal. This process has produced the fastest silicon devices to date, but requires a highly critical realignment to the initial polysilicon gate, which if not successful, would result in shorting the gate with the ohmic source/drain contacts. Therefore the above process is not compatible with manufacturing.

In addition to an increase in gate resistance due to scaling down the gate length in MOS FET's, the ohmic source/drain contacts formed by ion implantation cannot be scaled in depth as required to keep the aspect ratio of gate length to junction depth greater than 1. As the width of the MOS FET's are scaled, the resistance of the ohmic regions increases, which degrades the speed performance of the FETs. The threshold voltage has to be adjusted by a channel implant, which has to become shallower in order to prevent short channel effects. The shallower implant, in turn, reduces the carrier mobility in the inversion layer, and is also becoming more difficult to control.

Summary of the Invention

In accordance with the present invention, a structure and process sequence is described for building field effect transistors which can easily be scaled to submicron dimensions both in length and in width. The process relies on forming either Schottky metal ohmic source/drain contacts or raised, in-situ doped epitaxial ohmic contacts, and a metal or metal/polysilicon gate which is self aligned and may have a T-shape in order to reduce the parasitic gate resistance.

The invention provides a process for forming the gate stack, which allows a T-shaped metal gate with no critical alignment steps, and which results in a greatly reduced gate resistance.

The invention further provides a process which allows the formation of extremely shallow source/drain contacts, which are scalable in area.

The invention eliminates the need for gate stack silicon nitride sidewall spacers.

The invention further provides a new process that allows the formation of T-gates, self aligned to existing shallow source-drain contacts, without any critical alignment needed for example an alignment accuracy of about 0.2 μm for a gate length in the range

of 0.05 to 0.2μm.

The invention further provides a new alternative process where the gate is formed by metal or metal/polysilicon combination, without any silicidation needed, and results in an extremely low gate contact resistance.

The invention further provides a new process in which the source/drain contacts can be made by either a metal barrier or junction or an in-situ-doped semiconductor with respect to the channel, thus avoiding ion implantation and annealing. The high conductivity of the contacts described herein allows the scaling of the area of the contacts for high packing density circuits.

The invention further provides a self aligned raised epitaxial channel formed between raised semiconductor regions forming the source and drain.

The invention further provides a new process in which the same source/drain contact metal, for example titanium, can be selectively and locally oxidized to form the gate dielectric material, titanium dioxide, having a high dielectric constant, thus relaxing the scaling limits on the gate dielectric thickness.

Brief description of the Drawing

These and other features, objects, and advantages of the present invention will become apparent upon a consideration of the following detailed description of the invention when read in conjunction with the drawings, in which:

Fig. 1 is a cross section view illustrating early steps in forming the embodiment shown in Fig. 7.

Fig. 2 is a top view of the structure of Fig. 1 after the step of etching.

Fig. 3 is a cross section view along the line 3-3 of Fig. 2.

Figs. 4-6 are cross section views illustrating further steps in forming the embodiment shown in Fig. 7.

Fig. 7 is a cross section view of one embodiment of the invention.

Fig. 8 is a graph of the Drain-Source Current verses Drain-Source Voltage showing measurements made for the embodiment shown in Fig. 7.

Figs. 9-11 are cross section views illustrating the fabrication steps in forming the embodiment shown in Fig. 12.

Fig. 12 is a cross section view of a second embodiment of the invention.

Figs. 13-15 are cross section views illustrating the fabrication steps in forming the embodiment shown in Fig. 16.

Fig. 16 is a cross section view of a third embodiment of the invention.

Fig. 17 is a cross section view of a fourth embodiment of the invention.

Figs. 18 and 19 are cross section views illustrating process steps using ion implantation and for protecting the channel during ion implantation in forming the embodiment shown in Fig. 20.

Fig. 20 is a cross section view of a fifth embodiment of the invention.

Description of the Preferred Embodiments

Referring now to the drawing, Fig. 1 shows a cross section view of substrate 12, a sacrificial layer 14, a metal layer 16 which subsequently forms a Schottky barrier or junction with respect to the channel, and an insulating layer 18. Substrate 12 may be a single crystal semiconductor material suitable to form the channel of a MOS FET to be built. Substrate 12 may be, for example, silicon, silicon germanium, germanium, gallium arsenide, indium gallium arsenide, indium phosphide, and indium gallium arsenide phosphide. Sacrificial layer 14 is of a material which may be selectively etched with respect to substrate 12 and which may be consumed by Schottky metal layer 16, for example, in the form of a silicide or germanide. Sacrificial layer 14 functions to protect the channel from reactive ion etching (RIE) damage. Sacrificial layer 14 may be for example silicon germanium with a germanium content x where x is equal to or greater than 0.3 and the silicon content is 1-x. Sacrificial layer 14 may also be GaAs, InGaAs, InP, $In_{1-x}Ga_xAs_yP_{1-y}$ and Si. The material for metal layer 16 forms the source and drain of the MOS FET and is of a material having an appropriately selected work function. Metal layer 16 may be, for example, Co, Ni, Pd, Pt, Rh, Ta, Ti, W, combinations thereof and alloys thereof to provide a selected barrier height and may be blanket deposited by evaporation or sputtering. Metal layer 16 is then covered by insulating layer 18 which may be for example

a low temperature deposited oxide such as by CVD using tetra ortho ethyl silicate (TEOS) as the precursor.

Next, a resist is deposited on insulating layer 18 and lithographically patterned to define a gate window 19 and future source and drain regions as shown in Fig. 2. The gate window is opened through insulating layer 18 and metal layer 16 by using for example RIE. A trench is formed around future source and drain regions. Fig. 3 shows a cross section view along the line 3-3 of Fig. 2. Fig. 3 shows a sacrificial layer 14 over substrate 12 in gate window 19 such that the RIE damage does not reach the channel of the MOS FET to be built.

Next as shown in Fig. 4, metal layer 16 and sacrificial layer 14 underneath it are alloyed to form source and drain contacts 20 and 22 while not disturbing sacrificial layer 14 in gate window 19. Source and drain contacts 20 and 22 form Schottky barriers or junctions 23 and 24, respectively, with channel 25 in substrate 12 shown in Fig. 4. The ratio of thickness of metal layer 16 to sacrificial layer 14 and the temperature are adjusted to permit complete alloying of layer 14 to form Schottky source and drain junctions to the channel. There may be some alloying with substrate 12 at the original substrate 12 interface. The penetration of alloying into substrate 12 is slight and just enough to remove the heterojunction of sacrificiaal layer 14 and substrate 12. For example, sacrificial layer 14 may be SiGe, substrate 12

may be Si, and Schottky metal layer 16 may be Ti for a n channel FET. Upon the step of siliciding which may occur at a temperature at or above 600°C, a silicide or mixed silicide may be formed, for example, titanium silicide and titanium germanide. For a p channel FET, Schottky metal layer 16 may be for example Pt. Upon the step of siliciding at or above 250°C, platinum silicide and platinum germanide may be formed.

Next as shown in Fig. 5, a gate oxide 26 is formed or grown on substrate 12 in gate window 19, sidewalls 27 and 28 of gate window 19 and the upper surface of insulating layer 18. Gate oxide 26 may have a thickness in the range from 2 to 20 and typically 3 to 5 nm.

Referring to Fig. 6, a gate material 30 which may be, for example, Al, W, with or without appropriate diffusion barriers and with or without polysilicon underneath is either blanket deposited or grown over gate oxide 26 and patterned lithographically to define a T-shaped gate 32. T-shaped gate 32 extends over sacrificial layer 14 above gate oxide 26. A negative resist may be used in the process of patterning lithographically.

An insulating material 34 which may be, for example, silicon dioxide or a flowable oxide is formed over exposed gate oxide 26 and T-shaped gate 32. Holes or openings 35 may be opened through insulating material 34 as shown in Fig. 7. The holes or openings 35 may be subsequently filled with conductive material 36 for

example tungsten and planarized via chemical mechanical polish (CMP) to form vias co planar with the upper surface of insulating material 34 (not shown). Alternatively, a metal layer 37 may be formed filling holes 35 with conductive material 36 and forming a layer on insulating material 34. Metal layer 37 may be patterned to provide circuit interconnections.

Fig. 8 shows a graph of the drain-source current versus drain source voltage for the embodiment of Fig. 7 with a gate length of 0.25μm. The FET measured was an n channel with source contact 20 and drain contact 22 being a mixture of titanium silicide and titanium germanide formed by alloying a titanium layer 16 with a sacrificial layer of $SiGe_x$ where x is .3. The metal gate had a layer of Ti of 50 Angstroms and a layer of Al of 1500 Angstroms. The top or T length of the T shaped gate was 0.5μm. In Fig. 8 the ordinate represents drain-source current and the abscissa represents drain-source voltage. Curves 44-47 were plotted from measurements with the gate voltage at 0.5V, 1.0V, 1.5V and 2.0V respectively. The transconductance g_m was equal to about 210 mS/mm and output conductance g_d was equal to about 10 mS/mm.

Referring to Fig. 9, a cross section view is shown of the early steps of a process for forming the embodiment shown in Fig. 12. In Figs. 9-12, like references are used for functions corresponding to the apparatus of Figs. 1-7.

Referring again to Fig. 9, a semiconductor layer 40 is formed on substrate 12. Semiconductor layer 40 may be a single crystal or a polycrystalline material which can be selectively etched by way of a wet etch or RIE with respect to substrate 12. For example, substrate 12 may be silicon and semiconductor layer 40 may be silicon germanium alloy or vice versa or, substrate 12 may be GaAs and semiconductor layer 40 may be InGaAs or vice versa. Semiconductor layer 40 may be highly doped, for example, in the range from 5×10^{19} to 5×10^{20} atoms/cm3 and functions as the source and drain of the MOS FET shown in Fig. 12. Semiconductor layer 40 may be doped p-type for a p channel MOS FET and doped n-type for an n channel MOS FET. Semiconductor layer 40 may be epitaxially formed in-situ over substrate 12. Semiconductor layer 40 may then be covered by insulating layer 18 which may be for example an oxide formed at low temperature. Referring to Fig. 10, lithography is then used to open gate window 19 in insulating layer 18 and semiconductor layer 40 using for example, RIE.

Referring to Fig. 11, a gate oxide 26 is deposited in gate window 19 on substrate 12 and over the upper surface of insulating layer 18.

Referring to Fig. 12, a gate material 30 is formed over gate oxide 26 and patterned lithographically to define a T-shaped gate 32. Gate material 30 extends from gate window 19 over the upper surface of insulating layer 18 with or without gate oxide

therebetween. Gate oxide 26 may be removed over insulating layer 18 prior to depositing gate material 30.

Fig. 13 shows the early steps in forming an MOS FET shown in Fig 16. In Figs. 13-16 like references are used for functions corresponding to the apparatus of Figs. 1-7 and 9-12. Substrate 12 has on its upper surface metal layer 16 which may be any metal, for example, titanium or platinum. An insulating layer 18 which may be for example silicon nitride is formed on the upper surface of Schottky metal layer 16.

A gate window 19 is formed in insulating layer 18 as shown in Fig. 14. After opening gate window 19, metal layer 16 where exposed is oxidized to form for example TiO_2 which becomes gate dielectric 50 as shown in Fig. 15. If the temperature is kept below 700°C during oxidation then substrate 12 if silicon will not oxidize at the interface.

Next, a gate material 30 is formed over gate dielectric 50 and patterned lithographically to define a T-shaped gate 32 as shown in Fig. 16.

In a variation shown in Fig. 17, after opening the gate window 19 in the Schottky metal layer 16 shown in Fig. 3 or in in-situ heavily doped layer 40 shown in Fig. 10, the sample or substrate 12 may be inserted in an epitaxial growth system, which can

selectively grow a required semiconductor such as Si or SiGe in gate opening 19 on substrate 12 to form channel 52 without growing a semiconductor on top of insulating layer 18 of silicon dioxide or silicon nitride or on gate dielectric 26. The epitaxial layer forming channel 52 results in a raised FET channel which is in electrical or actual contact from both sides by the source 41 and drain 42. Lattice strain can be introduced in channel 52 by growing a heterostructure such as Si/SiGe and/or graded compositions in order to make use of enhanced transport properties (e.g. mobility) as described in US Patent 5534713 which issued on July 9, 1996 to K. E. Ismail, a coinventor herein and F. Stern which is assigned (one half) to the assignee herein and which is incorporated herein by reference to show the formation of strained layers to increase mobility etc.

In Figs. 17-20, like references are used for functions corresponding to the apparatus of Figs. 1-7 and 9-16.

In another variation as shown in Figs. 18-20, an insulating layer 18 is first deposited on substrate 12 and then lithographically patterned to open or form gate window 19 in insulating layer 18 which may be for example silicon dioxide. Gate window 19 can be filled by metal for example Ti using resist lift off or by a semiconductor such as Ge using selective growth. In both cases the gate window is filled with material that is chosen such that it can stop the implanted species during implant of the

source and drain which are implanted through insulating layer 18 for forming shallow self aligned source region 54 and drain region 56. The window material which may be for example Ge as shown in Fig. 18 or Ti as shown in Fig. 19 can thus easily be selectively etched with respect to the semiconductor substrate 12 underneath, substrate 12 which may be for example Si or SiGe alloy or combinations thereof. Following an annealing step to activate the implant, gate oxide 26 is deposited and the rest of the process for forming the T-gate for the FET is done.

In all of the above proposed processes, the choice of the ohmic contacts and the gate metal, depends on the required threshold voltages and the device design. The work function of the metal used for source and drain contacts as shown, for example in Figs. 7 and 16, is a subject of optimization. The higher the Schottky barrier height between the metal and the semiconductor, the higher the series access resistance from source and drain contacts to the channel. On the other hand, electrons or holes overcoming this barrier have to be very energetic and hence have a high injection velocity and maintain this velocity under the gate. Highly-doped semiconductor source and drain contacts as shown in Fig. 12 have lower injection barriers but are also more resistive than metal contacts. Therefore, depending on the application and the threshold voltages required, one or the other processes shown above can be chosen to build corresponding FET's shown in Figs. 7, 12 and 16.

The invention described herein can be used in building field-effect transistors such as metal-semiconductor FET's, modulation-doped FET's, metal-oxide-semiconductor FET's and circuits. Compared to existing process steps of such FET's, the structure and process of this invention can result in a greatly reduced gate resistance, and extremely shallow ohmic contacts. The combination of the above two effects results in higher FET device and circuit speeds. The advantage of using a Schottky metal for example titanium or platinum for the source and drain which is self aligned to the channel of the FET, allows very high injection velocity of carriers into the channel, and also scaling down the transistor width and area, since the metal remains highly conducting until the size approaches the size of the grains, which may be more than three orders of magnitude smaller than the area used for the source and drain in state-of-the-art FET devices.

While there has been described and illustrated an FET structure and method of making self aligned Schottky metal silicide and/or germanide source and drain contacts and a T-shaped gate or a heavily doped semiconductor material as the source and drain with a T-shaped gate, it will be apparent to those skilled in the art that modifications and variations are possible without deviating from the broad scope of the invention which shall be limited solely by the scope of the claims appended hereto.

CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:

1. A method of forming a field effect transistor comprising the steps of:

selecting a substrate of single crystal semiconductor material,

forming a first sacrificial layer on said substrate,

forming a metal layer on said first sacrificial layer, said metal layer including material suitable for forming a Schottky metal-to-semiconductor barrier and having a selected work function,

forming an insulating layer over said metal layer,

forming a gate opening in said insulating layer and said metal layer,

heating said substrate, first sacrificial layer and said metal layer above a selected temperature for a time period to react said metal layer and said sacrificial layer to form a Schottky metal-to-semiconductor barrier on said substrate,

removing said sacrificial layer in said gate opening to expose said substrate,

forming a gate dielectric on said substrate in said gate opening and over the sidewalls of said opening,

forming a conductive layer on said gate dielectric in said gate opening, and

patterning said conductive layer to define a gate electrode,

said Schottky metal barrier on opposite sides of said gate electrode corresponding to the source and drain of said field effect transistor.

2. The method of claim 1 wherein said step of selecting said single crystal semiconductor material includes the step of selecting from the group consisting of GaAs, InGaAs, InP, $In_{1-x}Ga_xAs_yP_{1-y}$, Si and SiGe.

3. The method of claim 1 wherein said step of forming a first sacrificial layer includes the step of selecting from the group consisting of GaAs, InGaAs, InP, $In_{1-x}Ga_xAs_yP_{1-y}$, Si and SiGe.

4. The method of claim 1 wherein said step of forming a metal layer includes the step of selecting from the group consisting of Co, Ni, Pd, Pt, Rh, Ta, Ti and W.

5. The method of claim 1 wherein said step of forming a metal layer includes the step of forming a titanium layer and wherein said step of heating includes heating to a temperature above 700°C.

6. The method of claim 1 wherein said step of forming a metal layer includes the step of forming a platinum layer and wherein said step of heating includes heating to a temperature above 250°C.

7. The method of claim 1 wherein said step of forming a first sacrificial layer includes the step of forming a silicon germanium layer and wherein said step of heating includes heating to a temperature to form metal silicide and metal germanide to provide a Schottky barrier to the semiconductor substrate.

8. The method of claim 1 further including the step of forming source and drain contacts to said Schottky metal barrier on opposite sides of said gate electrode and wherein said step of forming a conductive layer includes forming said conductive layer

on said sidewalls of said opening.

9. A field effect transistor comprising:

a semiconductor substrate,

two spaced apart Schottky metal semiconductor compound regions forming a source and drain and defining a channel there between,

a first dielectric layer on said source and drain adjacent said channel,

a gate dielectric layer on said channel, and

a conductive layer on said gate dielectric to form a gate.

10. The field effect transistor of claim 9 wherein said metal semiconductor compound regions are selected from the group consisting of metal silicide, metal germanide, mixtures of metal silicide and metal germanide, and metal arsenide.

11. The field effect transistor of claim 9 wherein said conductive layer extends over said first dielectric layer to reduce the resistance of said gate.

12. The field effect transistor of claim 9 wherein said conductive layer extends over said first dielectric layer over a portion of the source and drain to form a T-shaped gate.

13. A method of forming a field effect transistor comprising the steps of:

selecting a substrate of single crystal semiconductor material,

forming a first layer of heavily doped semiconductor material compositionally different from said substrate to provide a different etching rate with respect to said substrate,

forming a second insulating layer,

forming an opening in said first and second layers for a gate,

forming a gate dielectric on said substrate in said opening and over the sidewalls of said opening,

forming a conductive layer on said gate dielectric in said gate opening and on said sidewalls of said opening, and

patterning said conductive layer to define a gate electrode,

said first layer on opposite sides of said gate electrode corresponding to the source and drain of said field effect transistor.

14. The method of claim 13 wherein said step of selecting said single crystal semiconductor material includes the step of selecting from the group consisting of GaAs, InGaAs, InP, $In_{1-x}Ga_xAs_yP_{1-y}$, Si and SiGe.

15. The method of claim 13 wherein said step of forming a first layer includes the step of forming a single crystal layer.

16. The method of claim 13 wherein said step of forming a first layer includes the step of forming a polycrystalline layer.

17 The method of claim 13 wherein said step of forming a first layer includes the step of selecting from the group consisting of

GaAs, InGaAs, InP, $In_{1-x}Ga_xAs_yP_{1-y}$, Si and SiGe.

18. The method of claim 13 wherein said step of forming a second layer includes the step of selecting from the group consisting of silicon dioxide and silicon nitride.

19. The method of claim 13 wherein said step of forming a conductive layer includes the step of forming over said insulating layer and wherein said step of patterning includes defining a gate electrode that extends on said sidewalls and over said insulating layer.

20. The method of claim 19 wherein said step of patterning includes defining a gate electrode that extends on said sidewalls and over said insulating layer over a portion of said source and drain to form a T-shaped gate.

21. The method of claim 13 further including the step of forming source and drain contacts to said first layer on opposite sides of said gate electrode.

22. A field effect transistor comprising:

a semiconductor substrate,

two spaced apart heavily doped semiconductor regions on said semiconductor substrate forming a source and drain and defining a channel in said substrate there between, said semiconductor regions compositionally different from said substrate to provide a selective etching rate for forming said spaced apart regions,

a first dielectric layer on said source and drain adjacent said channel,

a gate dielectric layer on said channel and on the sidewalls, and adjacent said channel on said two spaced apart semiconductor regions, and

a conductive layer on said gate dielectric over said channel forming a gate.

23. The field effect transistor of claim 22 wherein said heavily doped semiconductor regions include SiGe alloy.

24. A method of forming a field effect transistor comprising the steps of:

selecting a substrate of single crystal semiconductor material,

forming a metal layer on said substrate, said metal layer including material suitable for forming a Schottky metal-to-semiconductor barrier and having a selected work function,

forming an insulating layer over said metal layer,

forming a gate opening in said insulating layer to expose said metal layer,

heating said metal layer in said gate opening above a selected temperature for a time period in a gaseous ambient to react said metal layer and constituents in said gaseous ambient to form a gate dielectric in said gate opening on said substrate,

forming a conductive layer on said gate dielectric in said gate opening, and

patterning said conductive layer to define a gate electrode,

said Schottky metal-to-semiconductor barrier on opposite sides of said gate electrode corresponding to the source and drain of said

field effect transistor.

25. The method of claim 24 wherein said step of selecting said single crystal semiconductor material includes the step of selecting from the group consisting of silicon and silicon germanium.

26. The method of claim 24 wherein said step of forming a metal layer includes the step of selecting from the group consisting of Co, Ni, Pd, Pt, Rh, Ta, Ti and W.

27. The method of claim 24 wherein said step of forming a metal layer includes the step of forming a titanium layer and wherein said step of heating includes heating in a gaseous ambient including oxygen.

28. The method of claim 24 wherein said step of heating includes heating in a gaseous ambient selected to react with said metal of said metal layer to form a dielectric material.

29. The method of claim 1 wherein said step of heating includes heating to a temperature to form a Schottky metal semiconductor compound with the material of said substrate.

30. A field effect transistor comprising:

a semiconductor substrate,

two spaced apart metal-semiconductor compound regions forming a source and drain and defining a channel there between,

a first dielectric layer on said source and drain adjacent said channel,

a gate dielectric layer of local reacted metal of said metal used in said metal-semiconductor compound regions on said channel, and

a conductive layer on said gate dielectric to form a gate.

31. The field effect transistor of claim 30 wherein said conductive layer extends over said first dielectric layer to reduce the resistance of said gate.

32. The field effect transistor of claim 30 wherein said conductive layer extends over said first dielectric layer over a portion of the source and drain to form a T-shaped gate.

33. The field effect transistor of claim 30 wherein said gate dielectric layer includes TiO_2.

34. A method for making an FET comprising:

selecting a semiconductor substrate, having a layer of dielectric thereon,

etching a gate window in said layer of dielectric exposing said substrate,

selectively growing germanium on said substrate in said gate window wherein no germanium has grown on said layer of dielectric,

using the germanium as a mask, implanting shallow regions of dopant ions to form the source and drain,

removing said germaniun,

forming a gate oxide in said gate window,

forming a layer of conductive material on said gate oxide and on said layer of dielectric, and

patterning said layer of conductive material to form a gate.

35. A method for making an FET comprising:

selecting a semiconductor substrate, having a layer of dielectric thereon,

etching a gate window in said layer of dielectric exposing said substrate,

forming a layer of resist on said layer of dielectric and on said exposed substrate in said gate window, exposing and developing said resist to remove resist from said gate window to expose said substrate,

forming a blanket layer of titanium over said resist and on said exposed substrate in said gate window,

removing the remainder of said resist and titanium on said resist,

using the titanium as a mask, implanting shallow regions of dopant ions to form the source and drain,

removing said titanium,

forming a gate oxide in said gate window,

forming a layer of conductive material on said gate oxide and on said layer of dielectric, and

patterning said layer of conductive material to form a gate.

36. The method of claim 13 further including the step of forming an epitaxial layer of second semiconductor material on said substrate in said opening to provide a raised channel above said substrate prior to said step of forming a gate dielectric.

A Scalable MOS Field Effect Transistor

ABSTRACT OF THE INVENTION

A field effect transistor and method for making is described incorporating self aligned source and drain contacts with Schottky metal-to-semiconductor junction and a T-shaped gate or incorporating highly doped semiconductor material for the source and drain contacts different from the channel material to provide etch selectivity and a T-shaped gate or incorporating a metal for the source and drain contacts and the oxide of the metal for the gate dielectric which is self aligned. The invention overcomes the problem of self-aligned high resistance source/drain contacts and a high resistance gate electrode for submicron FET devices which increase as devices are scaled to smaller dimensions.

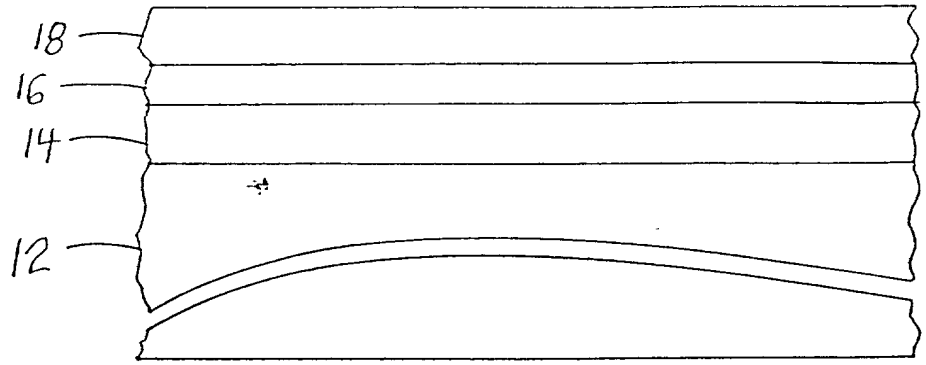


FIG 1

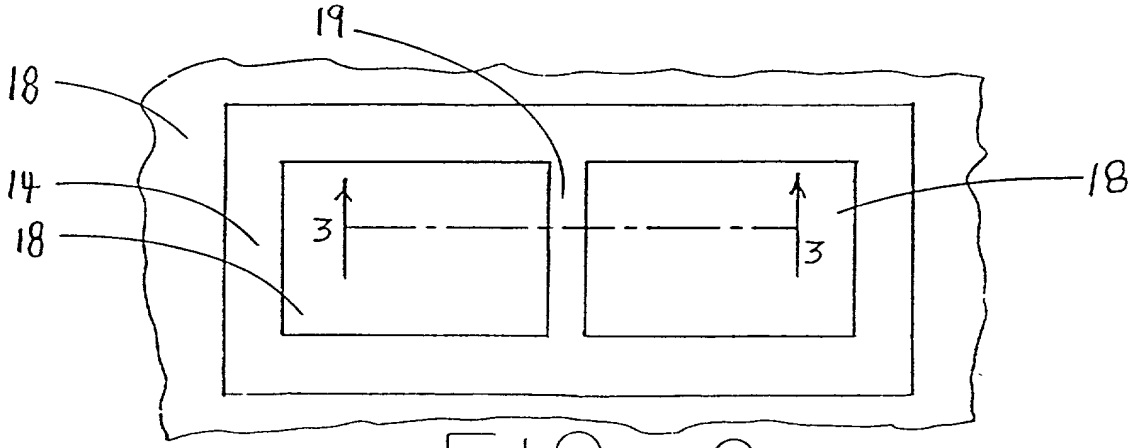


FIG 2

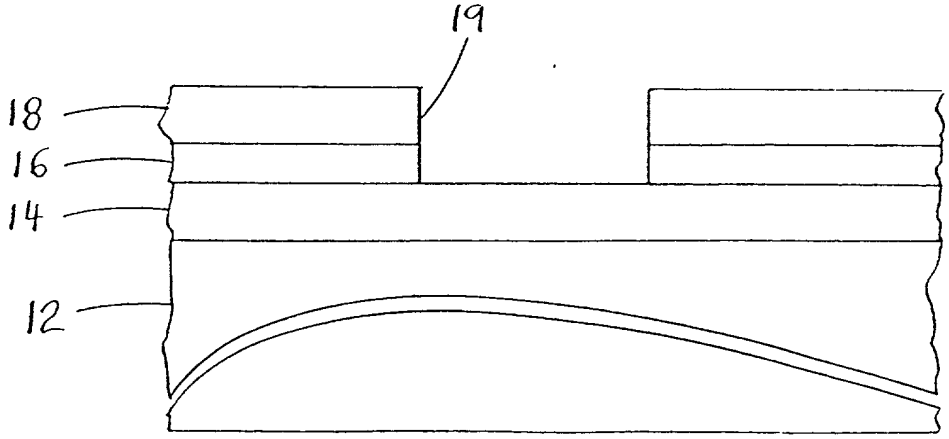


FIG 3

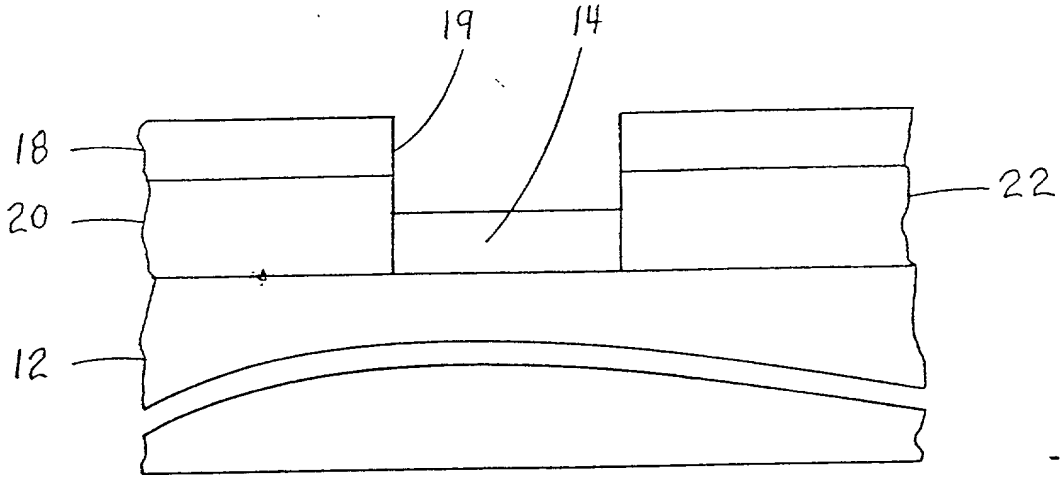


FIG 4

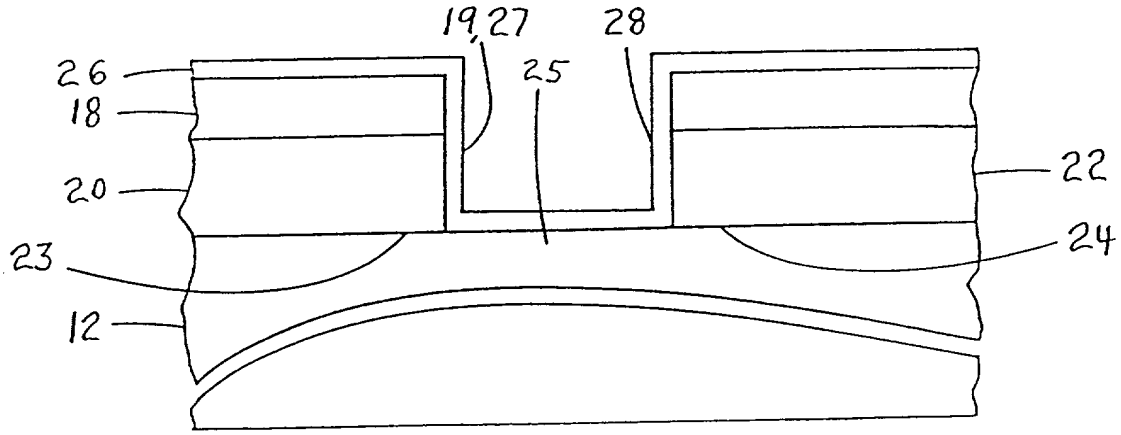


FIG 5

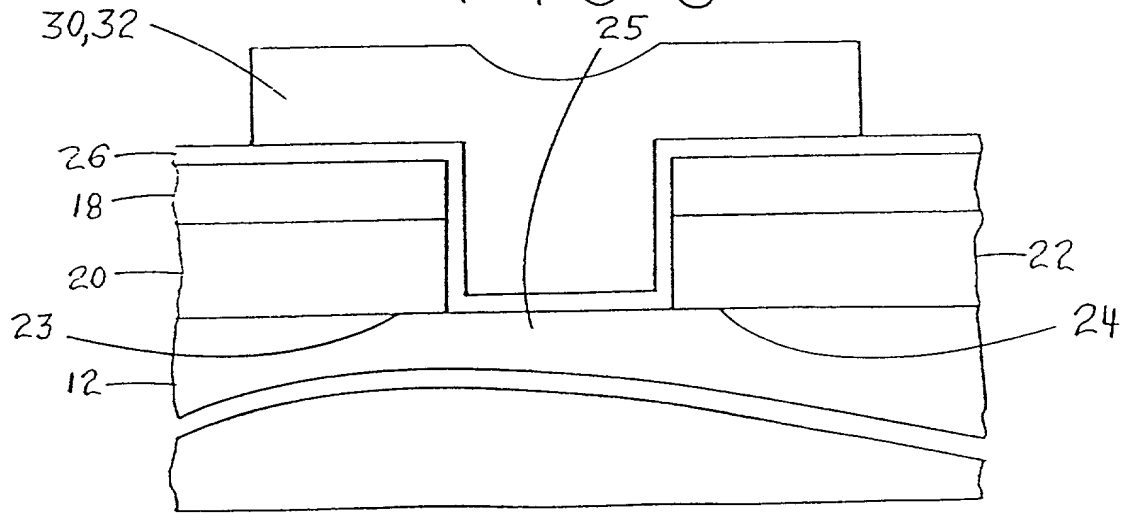


FIG 6

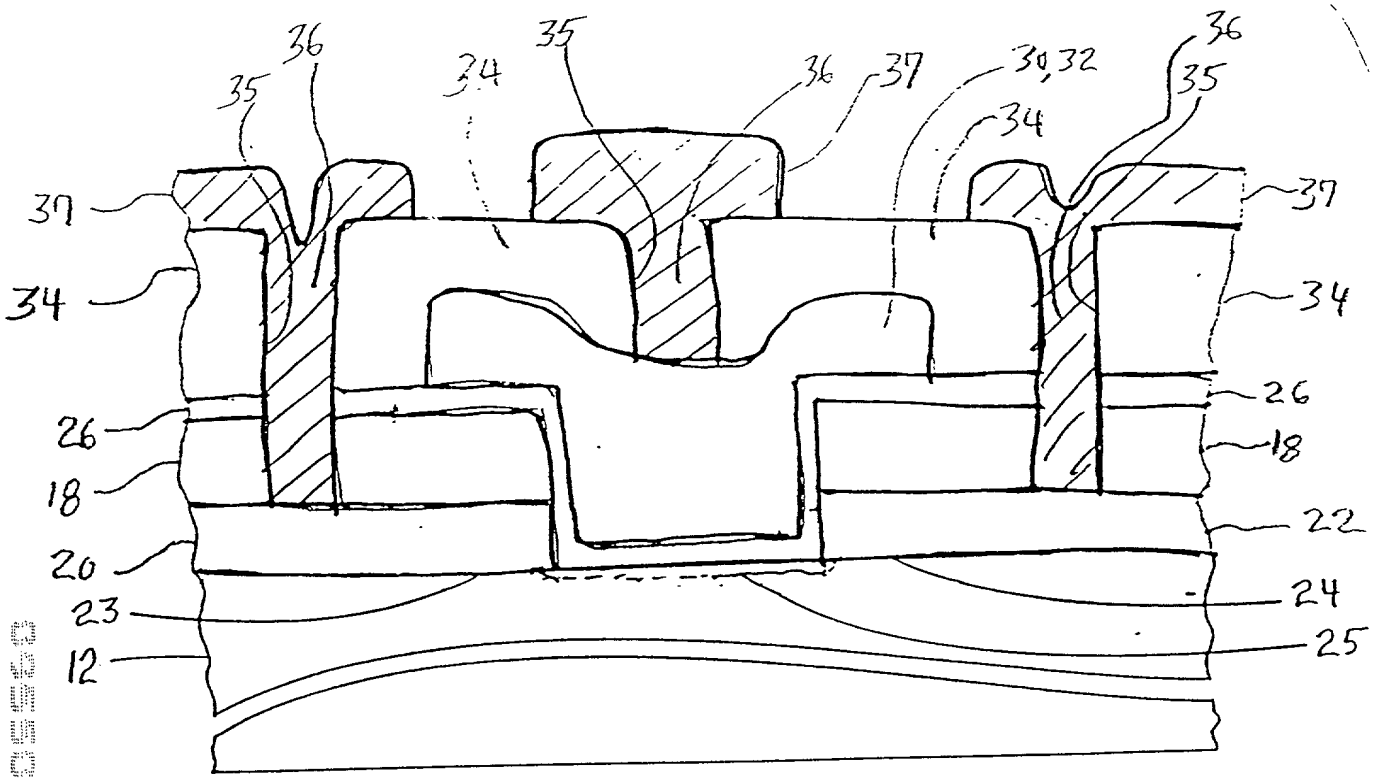
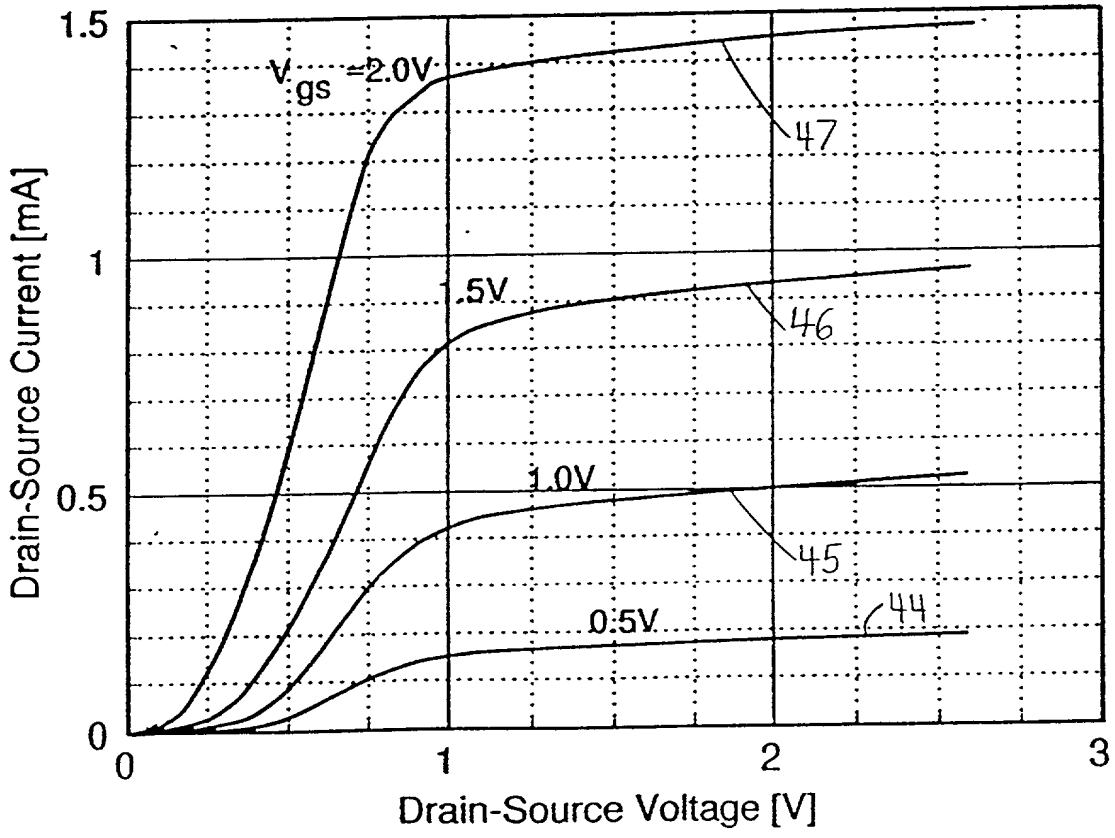


FIG 7



$g_{m_{max}} \approx 210 mS/m$
$g_d = 10 mS/m$

FIG 8

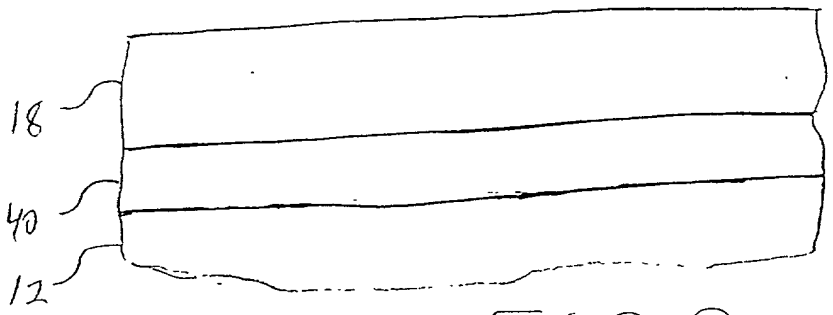


FIG 9

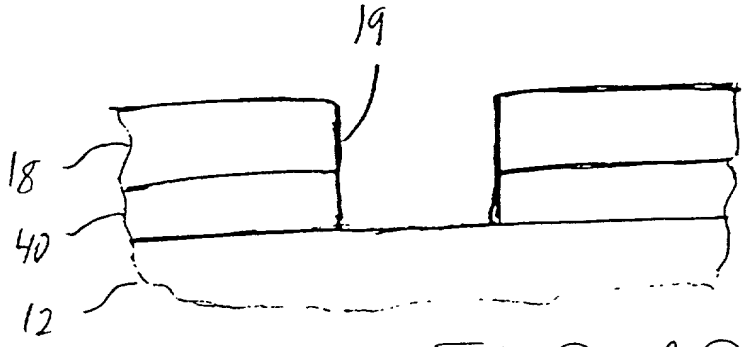


FIG 10

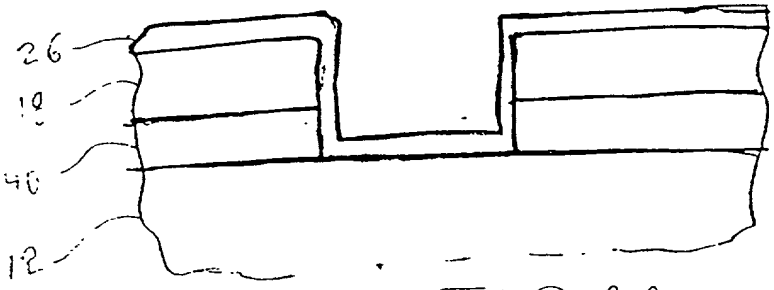


FIG 11

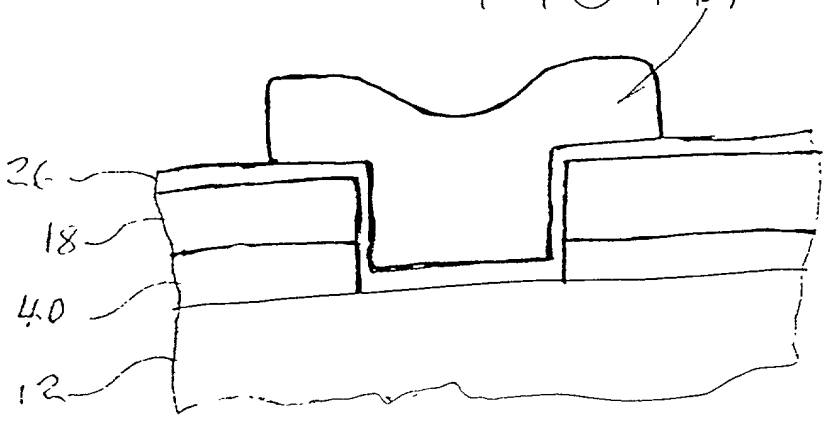


FIG 12

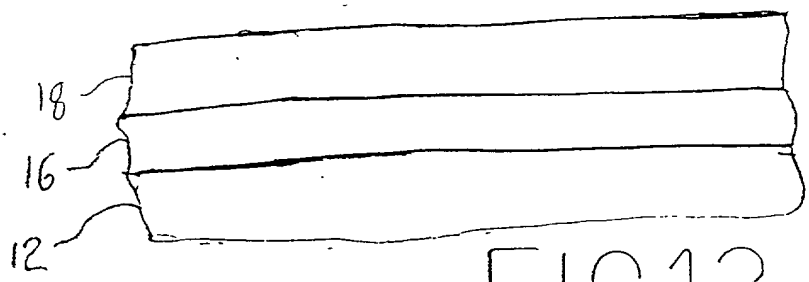


FIG13

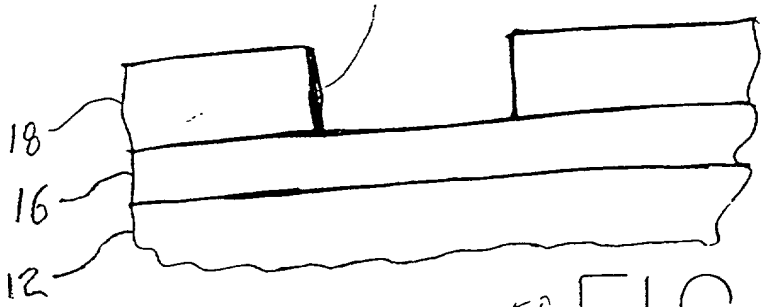


FIG 14

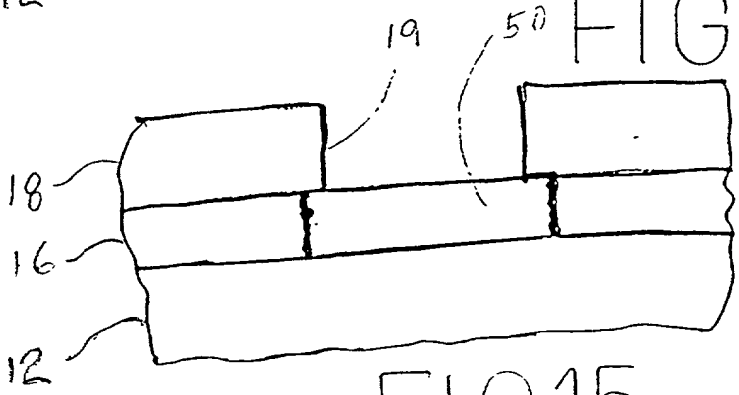


FIG15

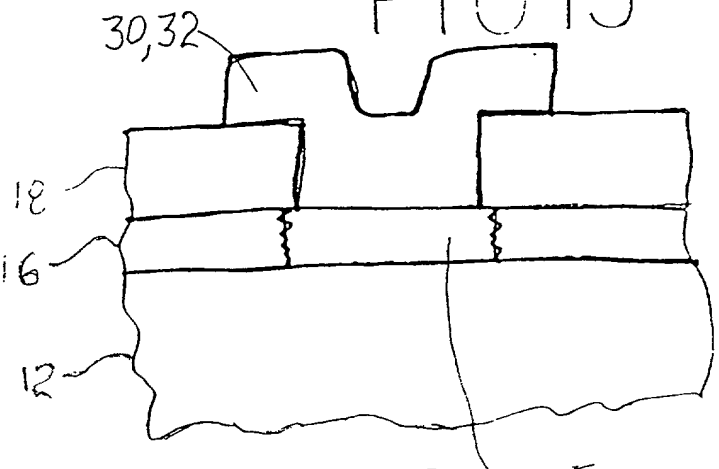


FIG16

Fig 17

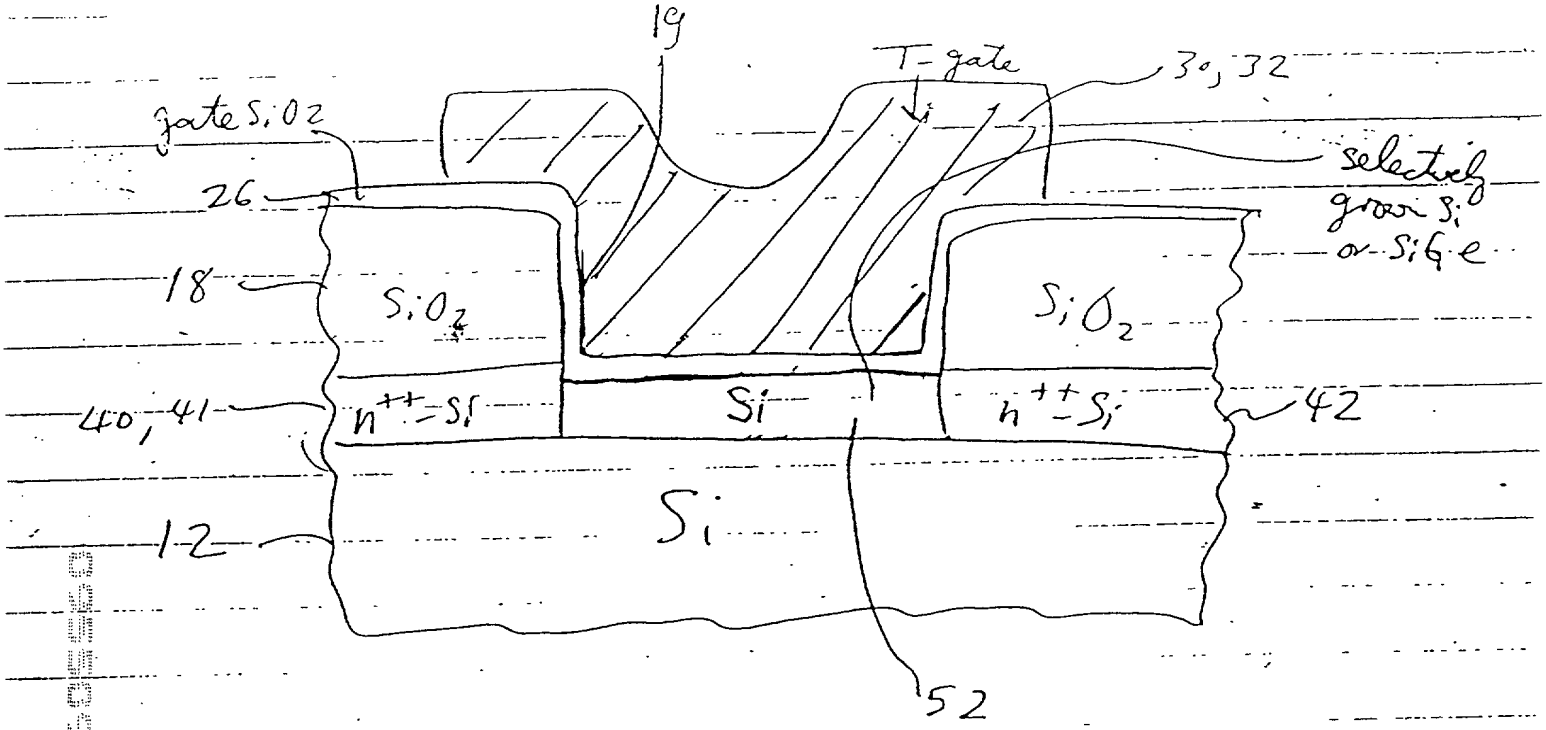


Fig 18

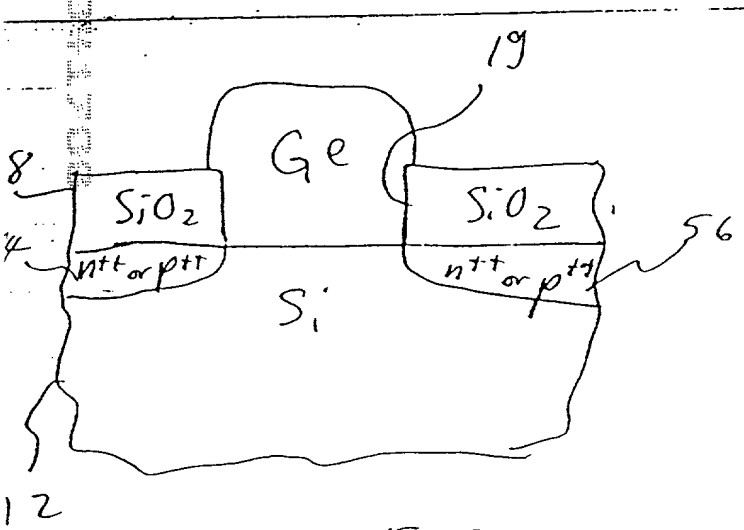


Fig 19

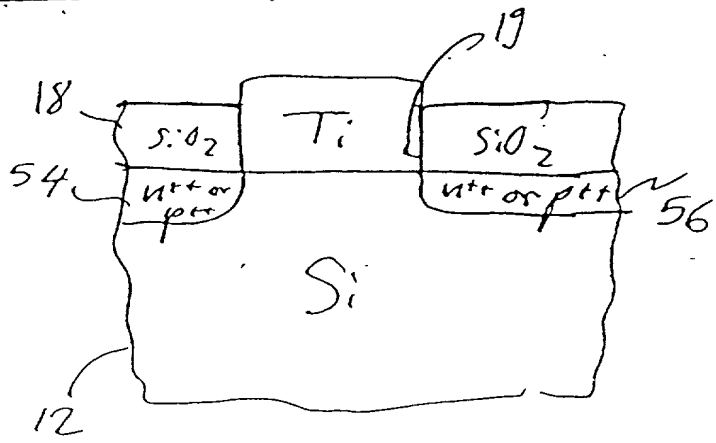


Fig 20

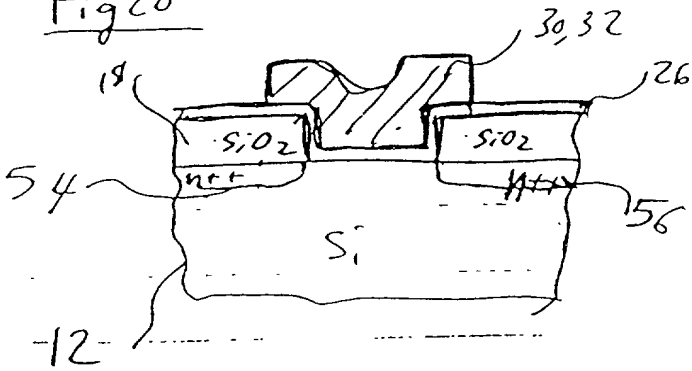


FIG 21

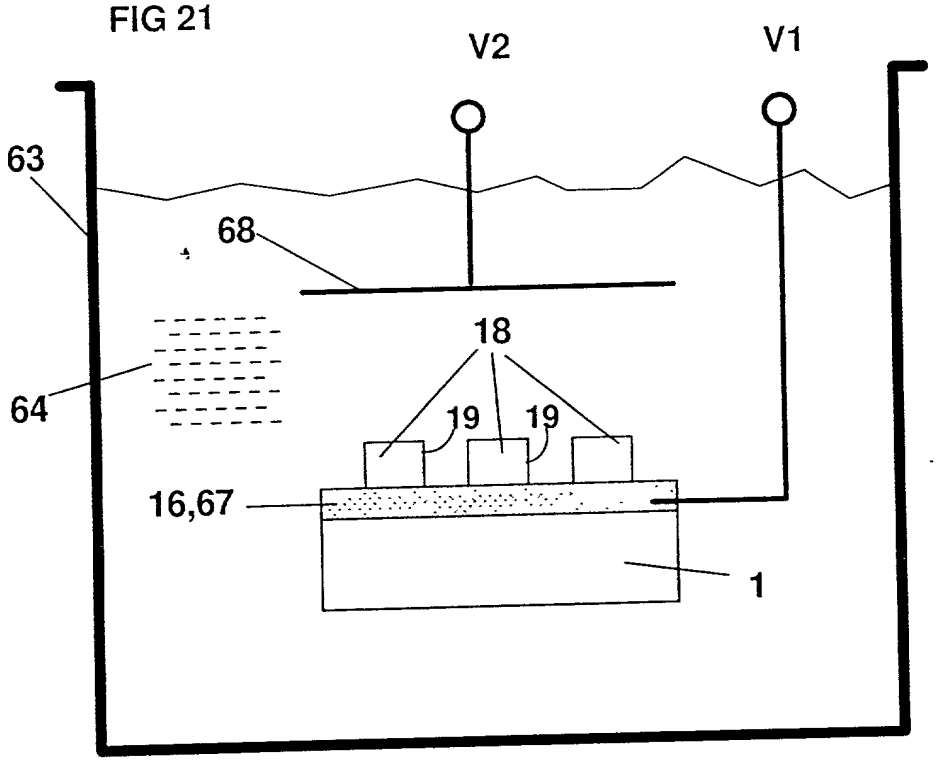


FIG 22

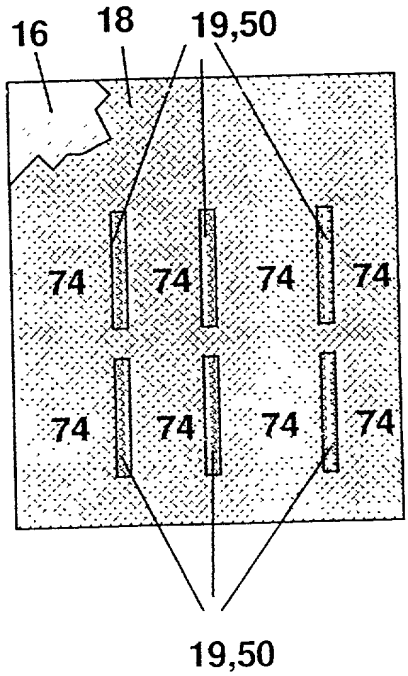


FIG 23

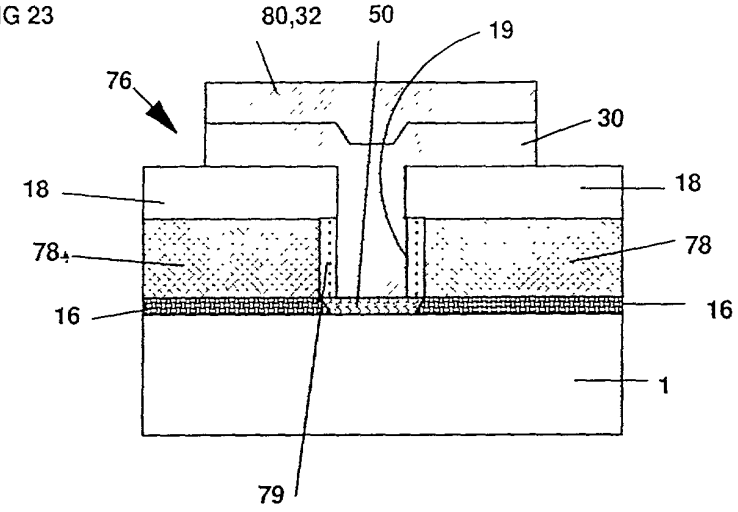


FIG 24

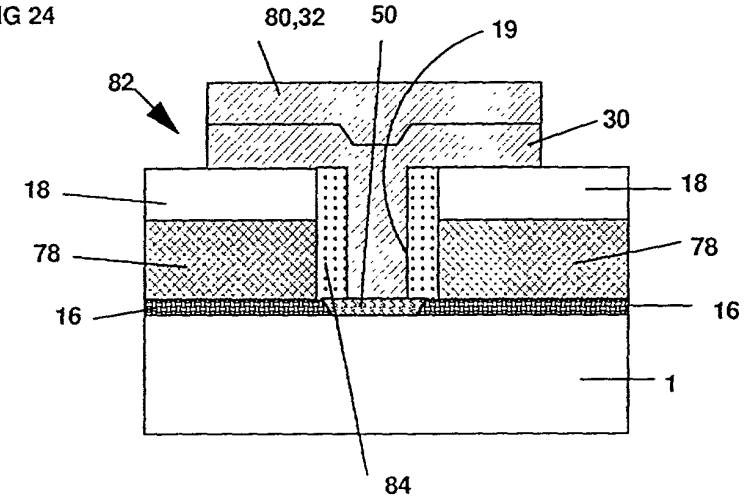
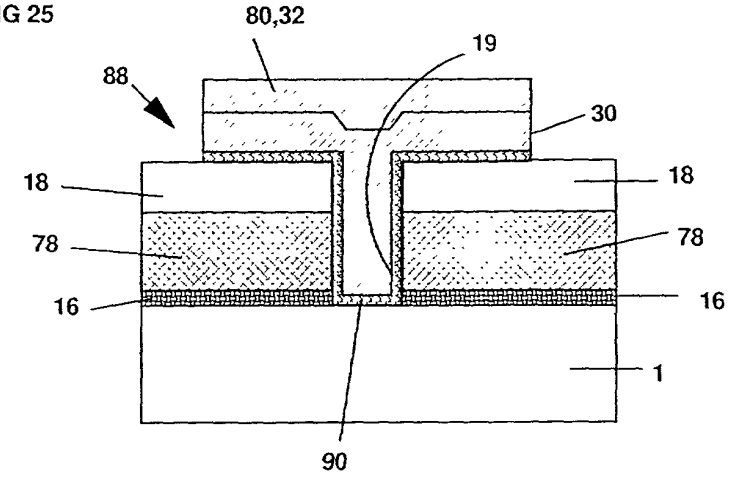


FIG 25



Docket No. YO996-118X

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

A SCALABLE MOS FIELD EFFECT TRANSISTOR

the specification of which (check one)

___ is attached hereto.

X was filed on June 30, 1998 as United States Application Number 09/107,738

or PCT International Application Number _____

and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application, having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	___ Yes ___ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	___ Yes ___ No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	___ Yes ___ No

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

_____ (Application Number)	_____ (Filing Date)
_____ (Application Number)	_____ (Filing Date)

I hereby claim the benefit under 35 U.S.C. §120 of any United States Application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States, or PCT International application in the manner provided by the first paragraph of 35 U.S.C. §112, I acknowledge the duty to disclose information material to the patentability of this application as defined in 37 CFR §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

08/683,329 (Application Serial No.)	July 18, 1996 (Filing Date)	Abandoned (Status) (patented, pending, abandoned)
_____ (Application Serial No.)	_____ (Filing Date)	_____ (Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number).

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Docket No. YO996-118X

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Citizenship

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